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EXAMINER	
CHU, WUTCHUNG	

ART UNIT	PAPER NUMBER
2619	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,774	PARKER ET AL.	
	Examiner	Art Unit	
	WUTCHUNG CHU	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 April 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This communication is in response to application's amendment filed on 5/19/2008. Claims 1-23 are pending.

Claim Rejections - 35 USC § 103

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Navada et al., hereinafter Navada, (US2003/0214956) in view of Kishnan (US2003/00225907).

Regarding claim 1, Navada discloses a method and apparatus for memory efficient east VLAN lookups and inserts in hardware-based packet switches **(see Navada paragraph 17 and paragraph 70 computer program)** comprising:

- A pointer to a sequence of one or more commands **(see Navada paragraph 54 where pointer memory location is read to determine if a data entry associated with the key is present, and if it is not the retrieval operation will ends otherwise is would stored in the pointer memory location is used to find the data entry in the first location, which corresponds to one ore more commands)**, for execution by a processor **(see Navada paragraph 50 processor)**, a first memory area **(see Navada paragraph 25 first table and figure 2 ref203)**; and
- a pointer to a burst of one or more data or mask items **(see Navada paragraphs 29 and 30)** for use by the one or more commands stored in a second memory **(see Navada paragraphs 25 and 30 second table and figure 2 ref205)** area distinct from the first **(see Navada paragraph 26 memories may also be stored in different arrangements)**.

Navada discloses all the subject matter of the claimed invention with the exception of:

- implementing one or more packet modification operations.

Kishnan from the same or similar fields of endeavor teaches the use of:

- routing engine, where the logical traffic identifier could be a tag inserted on top of the header or an identifier in a higher or lower OSI layer packet header **(see Kishnan paragraph 24 and figure 3 ref306 as corresponds to packet modification operation)**.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the routing engine which tags incoming packets with an logical identifier on top its headers, and it is implemented as a sparse array of pointers as taught by Krishnan in the apparatus for memory efficient east VLAN lookups and inserts in hardware-based packet switches of Navada in order to conserve valuable memory resources **(see Krishnan paragraph 10)**.

Regarding claim 2, Navada teaches the first and second memory areas are located in different memories **(see Navada paragraphs 26 memories may also be stored in different arrangements)**.

Regarding claim 3, Navada teaches the first and second memory areas are located in the same memory **(see Navada paragraphs 26 specific locations therein are substantially equivalent because tables used in omputing and networking devices are commonly implemented in memory)**.

Regarding claim 4, Navada disclose all the subject matter of the claimed invention with the exception of the one or more commands are stored in a packed format. Krishnan from the same or similar fields of endeavor teaches the use of routing engine is configured to obtain from the packet a key, a destination address, and a logical traffic identifier that indicates that the packet corresponds to a logical network **(see Krishnan paragraph 24)**.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the routing engine as taught by Krishnan in the apparatus for memory efficient east VLAN lookups and inserts in hardware-based packet switches of

Navada in order to conserve valuable memory resources **(see Krishnan paragraph 10)**.

Regarding claim 5, Navada teaches the one or more data or mask items **(see Navada paragraph 28 keys)** are stored in a packed format **(see Navada paragraphs 29 the content may also be obtained by substituting predetermined content for the actual content read by the reader, that is, by bit masking and/or by other methods that yield a reproducible content from a given key)**.

Regarding claim 6, Navada teaches the one or more data or mask items comprise data items **(see Navada paragraph data entry)** and associated mask items **(see Navada paragraph 62 key)**, with a data item stored adjacent to its associated mask item **(see Navada paragraph 62 a data entry associated with a key)**.

Regarding claim 7, Navada disclose all the subject matter of the claimed invention with the exception of the first and second memory areas are located in a memory implemented off chip from a modification processor configured to execute the one or more commands.

Krishnan from the same or similar fields of endeavor teaches the use of routing engine **(see figure 3 ref 306)** is configured to obtain from the packet a key, a destination address, and a logical traffic identifier. The routing engine could then be view as an processor which is off chip of the memory controller **(see Navada figure 2 ref215 and paragraph 25)**. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the routing engine as taught by Krishnan in the

apparatus for memory efficient east VLAN lookups and inserts in hardware-based packet switches of Navada in order to conserve valuable memory resources **(see Krishnan paragraph 10)**.

Regarding claim 8, Navada teaches the first memory area is located in a memory implemented on chip with the modification processor **(see Navada figure 2 ref215 memory controller)**.

Regarding claim 9, Navada teaches the data structure comprises one or more pointers **(see Navada paragraph 41 pointers)** and disclose all the subject matter of the claimed invention with the exception of each to a sequence of one or more commands implementing one or more packet modification operations. Kishnan from the same or similar fields of endeavor teaches the use of routing engine, which could tag a logical traffic identifier on top of the header or an identifier in a higher or lower OSI layer packet header. The logical network identification array may be implemented as a sparse array of pointers where a location in the array corresponds to a logical network **(see Kishnan paragraph 24 and figure 3 ref306)**.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the routing engine which tags incoming packets with an logical identifier on top its headers, and it is implemented as a sparse array of pointers as taught by Krishnan in the apparatus for memory efficient east VLAN lookups and inserts in hardware-based packet switches of Navada in order to conserve valuable memory resources **(see Krishnan paragraph 10)**.

Regarding claim 10, Navada teaches the data structure comprises one or more pointers **(see Navada paragraph 41 pointers)**, each to a burst of one or more data or mask items **(see Navada paragraph 30 a pointer for key with content"4" at the fourth location of the second table)**.

Regarding claim 11, Navada discloses a method and apparatus for memory efficient east VLAN lookups and inserts in hardware-based packet switches **(see Navada paragraph 17)** comprising:

- retrieving from a memory a data structure corresponding to the data structure index **(see Navada paragraph 34)**, and comprising a pointer to a sequence of one or more commands **(see Navada paragraph 54 where pointer memory location is read to determine if a data entry associated with the key is present, and if it is not the retrieval operation will ends otherwise is would stored in the pointer memory location is used to find the data entry in the first location, which corresponds to one ore more commands)**, for execution by a processor **(see Navada paragraph 50 processor)**,
- a pointer to a burst of one of more data or mask items for use by the one or more commands stored in a second memory **(see Navada paragraphs 25 and 30 second table and figure 2 ref205)** area distinct from the first **(see Navada paragraph 26 memories may also be stored in different arrangements)**;
- retrieving from the first memory area the one or more commands **(see Navada paragraph 34)**;

- retrieving from the second memory area the one or more data or mask items for use by the one or more commands **(see Navada paragraph 34)**; and
- executing the one or more commands **(see Navada paragraph 54 where pointer memory location is read to determine if a data entry associated with the key is present, and if it is not the retrieval operation will ends otherwise is would stored in the pointer memory location is used to find the data entry in the first location, which corresponds to one ore more commands)**, for execution by a processor **(see Navada paragraph 50 processor)** by the processor,

Navada discloses all the subject matter of the claimed invention with the exception of:

- implementing one or more packet modification operations and stored in a first memory area;
- thereby performing one or more packet modification operations on the packet.

Kishnan from the same or similar fields of endeavor teaches the use of:

- routing engine, where the logical traffic identifier could be a tag inserted on top of the header or an identifier in a higher or lower OSI layer packet header **(see Kishnan paragraph 24 and figure 3 ref306 as corresponds to packet modification operation)**.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the routing engine which tags incoming packets with an logical identifier

on top its headers, and it is implemented as a sparse array of pointers as taught by Krishnan in the apparatus for memory efficient east VLAN lookups and inserts in hardware-based packet switches of Navada in order to conserve valuable memory resources **(see Krishnan paragraph 10)**.

Regarding claim 14, Navada teaches the first and second memory areas are located in different memories **(see Navada paragraphs 26 memories may also be stored in different arrangements)**.

Regarding claim 15, Navada teaches the first and second memory areas are located in the same memory **(see Navada paragraphs 26 specific locations therein are substantially equivalent because tables used in omputing and networking devices are commonly implemented in memory)**.

Regarding claim 16, Navada disclose all the subject matter of the claimed invention with the exception of the one or more commands are stored in a packed format. Krishnan from the same or similar fields of endeavor teaches the use of routing engine is configured to obtain from the packet a key, a destination address, and a logical traffic identifier that indicates that the packet corresponds to a logical network **(see Krishnan paragraph 24)**.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the routing engine as taught by Krishnan in the apparatus for memory efficient east VLAN lookups and inserts in hardware-based packet switches of Navada in order to conserve valuable memory resources **(see Krishnan paragraph 10)**.

Regarding claim 17, Navada teaches the one or more data or mask items **(see Navada paragraph 28 keys)** are stored in a packed format **(see Navada paragraphs 29 the content may also be obtained by substituting predetermined content for the actual content read by the reader, that is, by bit masking and/or by other methods that yield a reproducible content from a given key)**.

Regarding claim 18, Navada teaches the one or more data or mask items comprise data items **(see Navada paragraph data entry)** and associated mask items **(see Navada paragraph 62 key)**, with a data item stored adjacent to its associated mask item **(see Navada paragraph 62 a data entry associated with a key)**.

Regarding claim 19, Navada disclose all the subject matter of the claimed invention with the exception of the first and second memory areas are located in a memory implemented off chip from a modification processor configured to execute the one or more commands.

Krishnan from the same or similar fields of endeavor teaches the use of routing engine **(see figure 3 ref 306)** is configured to obtain from the packet a key, a destination address, and a logical traffic identifier. The routing engine could then be view as an processor which is off chip of the memory controller **(see Navada figure 2 ref215 and paragraph 25)**. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the routing engine as taught by Krishnan in the apparatus for memory efficient east VLAN lookups and inserts in hardware-based packet switches of Navada in order to conserve valuable memory resources **(see Krishnan paragraph 10)**.

Regarding claim 20, Navada teaches the first memory area is located in a memory implemented on chip with the modification processor **(see Navada figure 2 ref215 memory controller)**.

Regarding claim 21, Navada teaches the data structure comprises one or more pointers **(see Navada paragraph 41 pointers)** and disclose all the subject matter of the claimed invention with the exception of each to a sequence of one or more commands implementing one or more packet modification operations. Kishnan from the same or similar fields of endeavor teaches the use of routing engine, which could tag a logical traffic identifier on top of the header or an identifier in a higher or lower OSI layer packet header. The logical network identification array may be implemented as a sparse array of pointers where a location in the array corresponds to a logical network **(see Kishnan paragraph 24 and figure 3 ref306)**.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the routing engine which tags incoming packets with an logical identifier on top its headers, and it is implemented as a sparse array of pointers as taught by Krishnan in the apparatus for memory efficient east VLAN lookups and inserts in hardware-based packet switches of Navada in order to conserve valuable memory resources **(see Krishnan paragraph 10)**.

Regarding claim 22, Navada teaches the data structure comprises one or more pointers **(see Navada paragraph 41 pointers)**, each to a burst of one or more data or mask items **(see Navada paragraph 30 a pointer for key with content"4" at the fourth location of the second table)**.

Regarding claim 23, Navada discloses a method and apparatus for memory efficient east VLAN lookups and inserts in hardware-based packet switches **(see Navada paragraph 17)** comprising:

- a step for retrieving from a memory a data structure corresponding to the data structure index **(see Navada paragraph 34)**, and a pointer to a sequence of one or more commands **(see Navada paragraph 54 where pointer memory location is read to determine if a data entry associated with the key is present, and if it is not the retrieval operation will ends otherwise is would stored in the pointer memory location is used to find the data entry in the first location, which corresponds to one ore more commands)**, for execution by a processor **(see Navada paragraph 50 processor),**
- a pointer to a burst of one of more data or mask items for use by the one or more commands stored in a second memory **(see Navada paragraphs 25 and 30 second table and figure 2 ref205)** area distinct from the first **(see Navada paragraph 26 memories may also be stored in different arrangements)**;
- a step for retrieving from the first memory area the one or more commands **(see Navada paragraph 34)**;
- a step for retrieving from the second memory area the one or more data or mask items for use by the one or more commands **(see Navada paragraph 34)**; and
- a step for executing the one or more commands **(see Navada paragraph 54 where pointer memory location is read to determine if a data entry associated with the key is present, and if it is not the retrieval operation will**

ends otherwise is would stored in the pointer memory location is used to find the data entry in the first location, which corresponds to one ore more commands), by the processor **(see Navada paragraph 50 processor)**,

Navada discloses all the subject matter of the claimed invention with the exception of:

- implementing one or more packet modification operations and stored in a first memory area;
- thereby performing one or more packet modification operations on the packet.

Kishnan from the same or similar fields of endeavor teaches the use of:

- routing engine, where the logical traffic identifier could be a tag inserted on top of the header or an identifier in a higher or lower OSI layer packet header **(see Kishnan paragraph 24 and figure 3 ref306 as corresponds to packet modification operation)**.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the routing engine which tags incoming packets with an logical identifier on top its headers, and it is implemented as a sparse array of pointers as taught by Krishnan in the apparatus for memory efficient east VLAN lookups and inserts in hardware-based packet switches of Navada in order to conserve valuable memory resources **(see Krishnan paragraph 10)**.

Response to Arguments

5. Applicant's arguments, see applicant's remark on page, filed 5/19/2008, with respect to objection to abstract, objection to drawing, and 101 rejection on claims 1-10 have been fully considered and are persuasive. The objection to abstract, objection to drawing, and 101 rejection of claims 1-10 has been withdrawn.

6. Applicant's arguments filed 5/19/2008 have been fully considered but they are not persuasive.

With regard to applicant's remark for claims 1, 11, and 23 (pages 8-10), applicant submits that the Navada and Krishnan perform the same function and thus no reason to combine, and 103 rejection fails to correspond to 1) to a sequence of one or more commands; 2) for execution by a processor; that 3) implement one or more packet modification operations.

However, Navada teaches a sequence of one or more commands in paragraph 54 where pointer memory location is read to determine if a data entry associated with the key is present, and if it is not the retrieval operation will ends otherwise is would stored in the pointer memory location is used to find the data entry in the first location, which corresponds to one ore more commands. Navada also teaches a processor for executing function in paragraph 50. And Kishnan teaches packet modification operation which the logical traffic identifier could be a tag inserted on top of the header or an identifier in a higher or lower OSI layer packet header in paragraph 24, and it would have been obvious to one of ordinary skill in the art at the time of the invention to

include inserting identifier in order to conserve valuable memory resources, and thus meet all limitations and rejection respectfully remains.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shiga et al. (US2005/0044199)

Kadambi et al. (US2004/0174898)

Schwartz et al. (US6185214)

Nelson (US6292838)

Malalur (US6842457)

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WUTCHUNG CHU whose telephone number is (571)270-1411. The examiner can normally be reached on Monday - Friday 1000 - 1500EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571 272 7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/WC/
Wutchung Chu

/Edan Orgad/

Supervisory Patent Examiner, Art Unit 2619